UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,995	01/09/2006	Andrea Milanesi	DE03 0240 US1	7025

65913 7590 12/08/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
MORRIS, JOHN J	
ART UNIT	PAPER NUMBER
4147	

NOTIFICATION DATE	DELIVERY MODE
12/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/563,995	MILANESI, ANDREA	
	Examiner	Art Unit	
	JOHN J. MORRIS	4147	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/09/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5, 7, 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huijsing et al. (US Pat# 5734297/ *or "Huijsing" hereinafter*).

For **claim 1,** Huijsing teaches an apparatus comprising an input stage with an NMOS transistor doublet having a first differential input for receiving input signals and a PMOS transistor doublet having a second differential input for receiving input signals (Huijsing, figure 1). Huijsing also teaches constant transconductance (Huijsing, column 4, lines 11-54, figure 2 and 3). Huijsing does not teach a switching means; however, the examiner takes an official notice that it was well known in the art that at least one analog demultiplexer could receive and selectively direct analog input signals to either input wherein the demultiplexer is controlled by a switching signal. It would have been obvious to modify Huijsing because the use of a demultiplexer could easily switch between signals.

For **claim 2,** it is well known in the art to control a demultiplexer based on the voltage level of a signal. Therefore, one could select to direct the input signals to the first differential input if the input signals have an LC voltage above VCOM (e.g. positive gamma data) and to second differential input if the input signals have an LC voltage lower then VCOM (e.g. negative gamma data).

For **claim 3,** Huijsing teaches the NMOS transistor doublet comprises two NMOS transistors, each having a gate, whereby the gate of the first of the two NMOS transistors is connectable to a first input node and the gate of the second of the two NMOS transistors is connectable to a second input node, the PMOS transistor doublet comprises two PMOS transistors, each having a gate, whereby the gate of the first of the two PMOS transistors is connectable to the first input node and the gate of the second of the two PMOS transistors is connectable to the second input node (Huijsing, figure 1).

For **claim 5**, Huijsing teaches a rail-to-rail input stage (Huijsing, column 2, lines 17-18).

For **claim 7,** it would have been an obvious matter of design choice to use a digital signal to control the switching circuit since the signal only needs to have two states, on and off.

For **claim 9,** Huijsing teaches transistor doublets as part of a folded cascade rail-to-rail input stage and wherein the folded cascade rail-to-rail input stage is connected to a second stage comprising a rail-to-rail output stage amplifier (Huijsing, figure 1 and 6).

For **claim 10,** it would have been an obvious matter of design choice to have a plurality of apparatus' in a driver bank since such a modification would only require a mere replication of the apparatus. It is also well known that a bus is used for receiving input signals since a bus may only be an electrical connection use to transfer data.

For **claim 12,** it was well known in the art that a signal generator would be needed to generate the switching signals, or else the apparatus would not work correctly.

3. Claims 4, 8, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huijsing et al. (US Pat# 5734297/ *or "Huijsing" hereinafter*) in view of Miyazawa et al. (US Pub# 20020196247 A1/ *or "Miyazawa" hereinafter*).

For **claim 4,** Huijsing does not teach the gates of the transistors being connected to the same node; however, in the same field of endeavor, Miyazawa teaches MOS transistor doublets wherein the gates of the first doublet are connected to a first node and the gates of the second doublet are connected to a second node (Miyazawa, figure 1, items M5, M6, phi3, M2, M4, and phi2). Miyazawa teaches that these transistors can be either NMOS or PMOS (Miyazawa, page 4, paragraph [0049], lines 1-5). It would have

been obvious to one of ordinary skill in the art at the time the invention was made to modify Huijsing with Miyazawa. This is so because Huijsing teaches a rail-to-rail input stage with constant transconductance circuit and the applicant teaches that it is prior art to use rail-to-rail input stage circuits as part of LCD source drivers. Miyazawa also teaches part of a display driver circuit. Therefore both teach related subject matter and the modification would allow for an increase in control as to which transistor pairs to use.

For **claim 8,** Miyazawa teaches using transistors as switches (Miyazawa, figure 1, page 3, paragraph [0041], lines 1-4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huijsing with Miyazawa. This is so because Huijsing teaches a rail-to-rail input stage with constant transconductance circuit and the applicant teaches that it is prior art to use rail-to-rail input stage circuits as part of LCD source drivers. Miyazawa also teaches part of a display driver circuit. Therefore both teach related subject matter and the modification would allow for an increase in control as to which transistor pairs to use.

For **claim 13,** Miyazawa teaches that the circuit is part of a display panel module (Miyazawa, page 5, paragraph [0063], lines 1-3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huijsing with Miyazawa. This is so because Huijsing teaches a rail-to-rail input stage with constant transconductance circuit and the applicant teaches that it is prior art to use rail-to-rail input stage circuits as part of LCD source drivers. Miyazawa also teaches part of a

display driver circuit. Therefore both teach related subject matter and the modification would allow for an increase in control as to which transistor pairs to use.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huijsing et al. (US Pat# 5734297/ *or "Huijsing" hereinafter*) in view of Miyazawa et al. (US Pub# 20020196247 A1/ *or "Miyazawa" hereinafter*) and applicant admitted prior art (*AAPA hereinafter*).

For **claim 11,** Huijsing teaches an apparatus comprising an input stage with an NMOS transistor doublet having a first differential input for receiving input signals and a PMOS transistor doublet having a second differential input for receiving input signals (Huijsing, figure 1). Huijsing also teaches constant transconductance (Huijsing, column 4, lines 11-54, figure 2 and 3). Huijsing does not teach a switching means; however, it was well known in the art that at least one analog demultiplexer could receive and selectively direct analog input signals to either input wherein the demultiplexer is controlled by a switching signal. Huijsing does not teach a gate driver bank or an LCD panel; however, in the same field of endeavor, AAPA teaches that it is prior art for a conventional LCD to comprise of a gate driver bank and an LCD panel (AAPA, figure 4). AAPA also teaches a standard rail-to-rail input stage circuit (which Huijsing teaches) used in LCD (AAPA, figure 3). Therefore, it would have been obvious to modify Huijsing to be included in a conventional LCD driver circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huijsing

with Miyazawa. This is so because Huijsing teaches a rail-to-rail input stage with constant transconductance circuit and the applicant teaches that it is prior art to use rail-to-rail input stage circuits as part of LCD source drivers. Miyazawa also teaches part of a display driver circuit. Therefore both teach related subject matter and the modification would allow for an increase in control as to which transistor pairs to use. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Huijsing and Miyazawa with AAPA because all deal with the same subject matter and the addition of the AAPA would increase the effectiveness of the gate driver.

5. Claims 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huijsing et al. (US Pat# 5734297/ *or "Huijsing" hereinafter*) in view of Schade, JR. (US Pat# 4392112/ *or "Schade" hereinafter*).

For **claim 6,** Schade teaches an amplifier circuit with a plurality of switches to selectively direct the input signals (Schade, figure 1, items S1 to S6). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Huijsing with Schade because both deal with the amplifiers and the addition of the switches would allow control of the input signals, which could be of benefit for a plurality of reason, one of which could be using the amplifier for audio, video signals, or data signals. This would also increase the versatility.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Huijsing et al. (US Pat# 4555673) discloses a differential amplifier with rail-to-rail input capability and controlled transconductance; Shah et al. (US Pub# 20020026552 A1) discloses system and method for switching signals over twisted-pair wires.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN J. MORRIS whose telephone number is (571)270-7171. The examiner can normally be reached on Monday - Friday 7am - 3pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kieu-Oanh Bui can be reached on (571)272-7291. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KIEU-OANH BUI/
Supervisory Patent Examiner, Art Unit 4147

JOHN J MORRIS
Examiner
Art Unit 4147